Amendments to the Specification

At page 7, following line 30, please insert the following new paragraph:

--FIG. 3 is a timing diagram showing a digital signal and a time constant which is shorter than the minimum period of the digital signal.--

At page 8, please replace the paragraph beginning at line 9 with the following rewritten paragraph:

--In the LVDS transmitter 1, a constant current of 3-4 mA is switched through a bridge circuit. At terminal resistor 3 there then results a differential signal of ±400 mV. However, the transfer lines 4 can have a particular line capacitance depending on the application site, which for example can be the connection of an integrated circuit with an integrated circuit or the connection of a circuit board with another circuit board. Together with the terminal resistor 3, this gives an RC time constant which limits the maximum speed or bit rate. So that the level can settle at the end value, the RC time constant should not exceed one-third of the signal duration. FIG. 3 is a timing diagram showing a digital signal and a time constant which is shorter than the minimum period of the digital signal. In FIG. 3, s is a general digital signal. A time constant τ is shorter than the minimum period of the digital signal s. --